DSG-NPS R&D Meeting Minutes

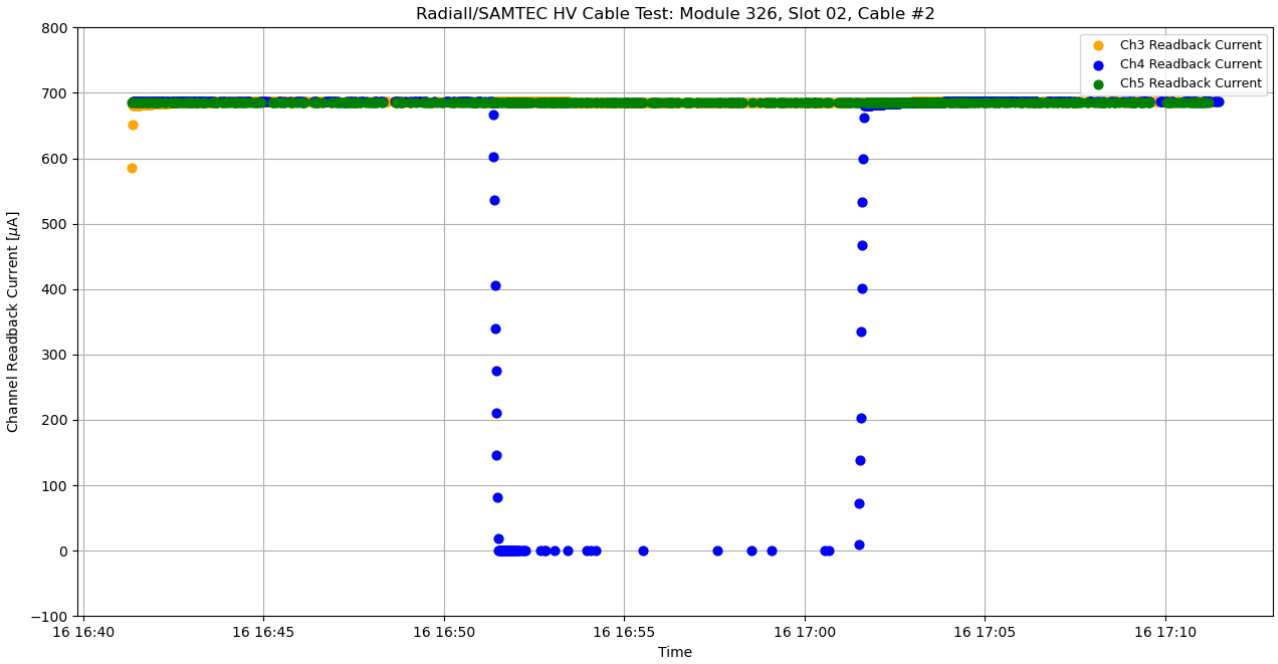
Date: April 20, 2021
Time: 11:00AM – 12:15 PM

Attendees: Peter Bonneau, Aaron Brown, Brian Eng, George Jacobs, Mindy Leffel, Marc McMullen, and Amrit Yegneswaran

1. HV supply cable fabrication and testing

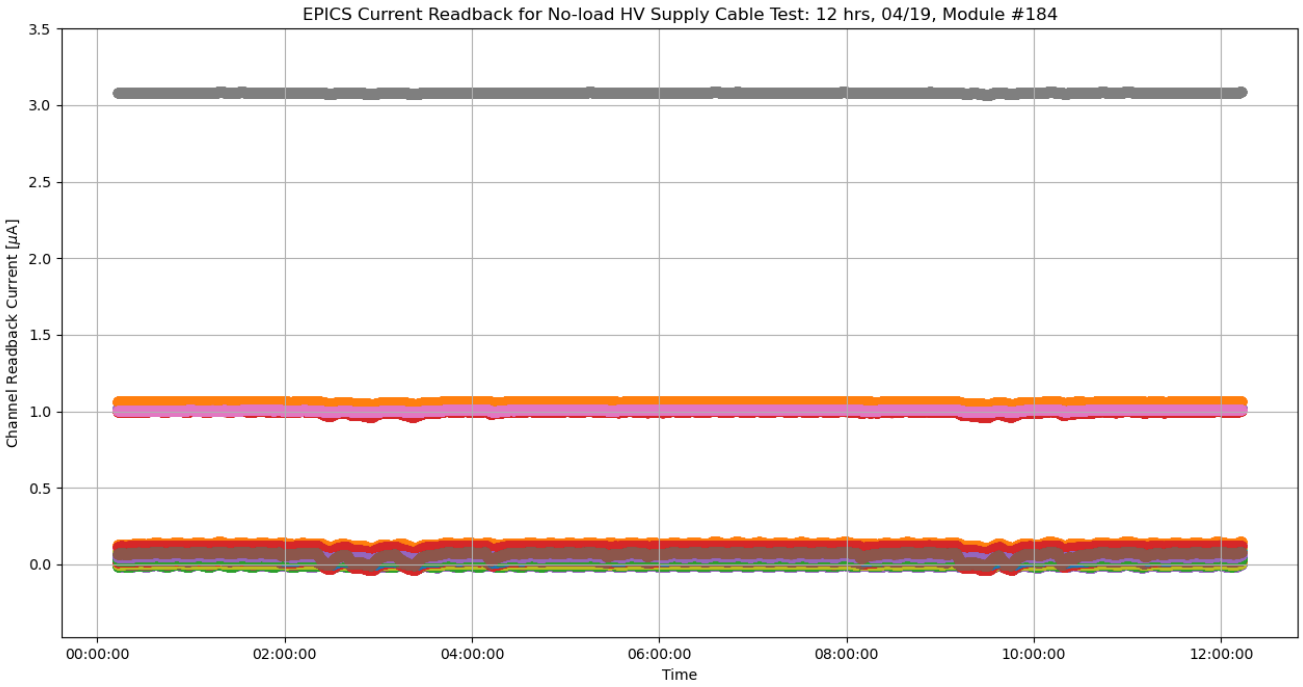
Peter Bonneau, Aaron Brown, Brian Eng, George Jacobs, Mindy Leffel, and Marc McMullen

1. Generated plots of 12-hour cable test (cable #2 in module #326)
    - Plots will be redone using a log scale for the *y*-axis
    - Goal is to zoom in to get separation between the three channels on either side of the ten-minute period when channel 4 (shown below) was turned off
    - In its current iteration, the two adjacent channels appear to have stable current for the entire time channel 4 was turned off; zooming in will allow for verification
    - Two minutes will be removed from both ends of the test period to avoid extraneous data points



Channel 4 of cable #2 switching test done on CAEN A7030TN module #326

2. EPICS current readback data was collected over 12 hours
    - Discussed possible reasons for one channel being well outside of maximum accuracy (±1% ±1μA) for the CAEN A7030TN HV module readback current
    - Contacted CAEN technical support regarding issue
    - Plot will be redone with text boxes to indicate the number of the channel that is out of specifications
    - A few individual channels will be plotted to get a clearer picture of how steady the current readback is for these channels



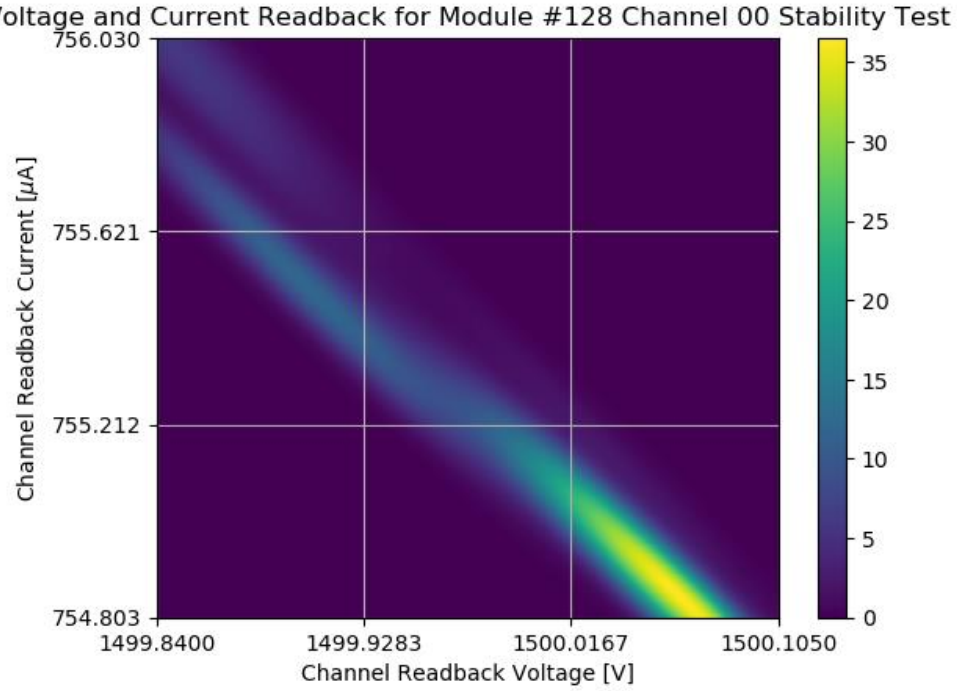
EPICS current readback data for all channels of module #184 shows one channel out of specifications

3. Discussed safety loop concerns regarding cable testing
    - The safety loop pin and the return pin on SAMTEC 3 were connected to allow for no-load testing of the cables
    - This connection will be removed for the load tests as safety loop connections are handled inside of the test chassis
    - Will review schematic for NPS HV board to be used in the detector to see if there are safety loops added to SAMTEC connectors 1 and 2
    - Will contact Carlos Munoz to inquire about safety loop concerns
4. Next step is to take data for module #184 while it is the only module in the crate
    - Will check if other modules have an effect on the module being monitored

2. Voltage and Current Density plots

Aaron Brown and George Jacobs

1. Revised the Python code for generating V and I density plots; reduced the number of *x*- and *y*-axis tick marks
2. It appears as if data points have been cut off for a few of the plots
3. Revisions to Python code will be done to increase the axes scales



Voltage and current density plot for module #128 channel #00

3. Hardware Interlock System development

Peter Bonneau

1. Reviewed procurement list for sensors and instrumentation for hardware interlock system